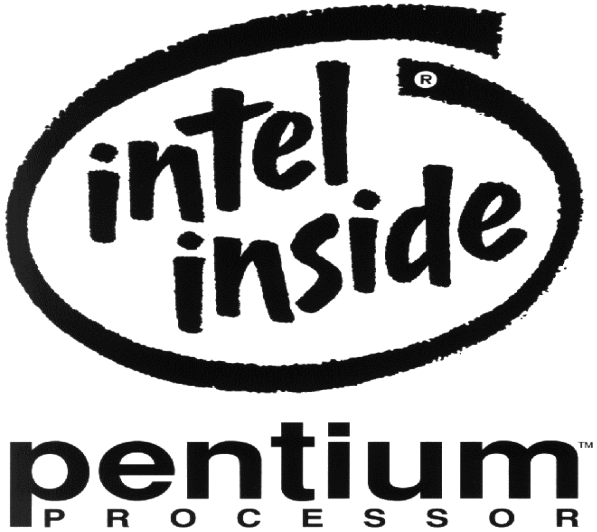
PC Architecture for Technicians: Level-1



Systems Manufacturing Training & Employee Development

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Chapter 1
Introduction
PC Architecture for Technicians: Level-1

Systems Manufacturing Training and Employee Development

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Where to get more information

- **The Indispensable PC Hardware Book (Messmer)**
  - Addison-Wesley (ISBN 0-201-87697-3)
- **ISA System Architecture (Shanley & Anderson)**
  - Mindshare (ISBN 0-201-40996-8)
- **The Personal Computer from the Inside Out**
  - Addison-Wesley (ISBN 0-201-62646-2)
- **The Peter Norton PC Programmer's Bible**
  - Microsoft Press (ISBN 1-55615-555-7)
- **The Indispensable Pentium™ Book (Messmer)**
  - Addison-Wesley (ISBN 0-201-87727-9)
- **Pentium™ Processor System Architecture**
  - Mindshare (ISBN 1-881609-07-3)

Where to get more information

- **Pentium™ Processor User's Manual**
  - Intel Order Number 241428
- **Pentium™ Architecture & Programming Manual**
  - Intel Order Number 241430
- **PCI Local Bus Specification (PCI SIG)**
  - PCI Special Interest Group (CC:Mail PCI_SIG)
- **PCI System Architecture (Shanley & Anderson)**
  - Mindshare (ISBN 0-201-40993-3)
- **PCI Hardware and Software (Solari & Willse)**
  - Annabooks (ISBN 0-929392-28-0)

This chapter provides an overview of concepts which will be covered in more detail throughout the course.

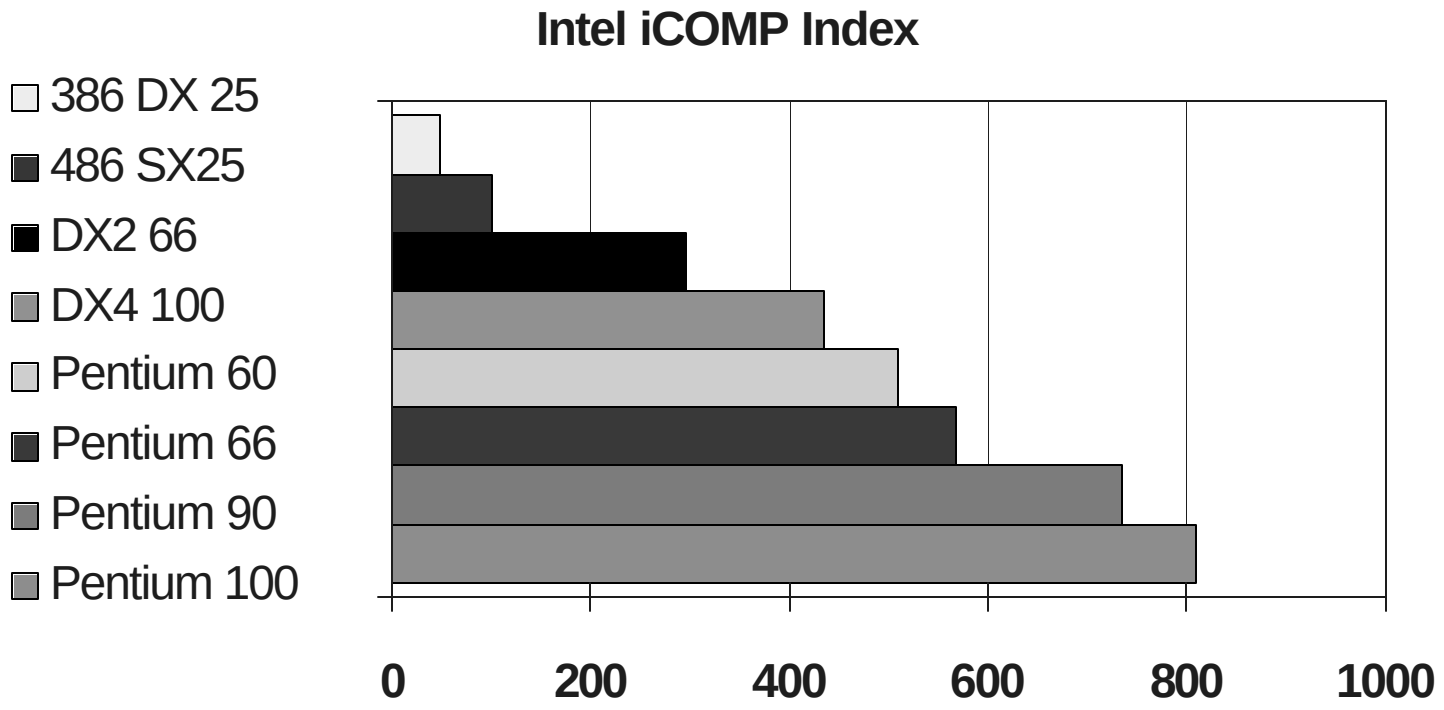
- The PC based on the Pentium™ is processor is compatible with entire installed base of applications for MS-DOS, OS/2, and UNIX.
- You will learn about PC architecture, signals and key bus cycles.
- The knowledge acquired here will serve a foundation for the boards based on Intel processors.

OBJECTIVES: At the end of this section, the student will be able to do the following:

- Discuss the **iCOMP**(TM) INDEX
- Discuss System Buses.
- Describe a simple Microprocessor System
- Describe the System Board & Peripheral chips.
- Discuss Microprocessor Buses & simple bus cycles.
- Discuss fetching of initial instructions after CPU is reset.

THE iCOMP(TM) INDEX

Intel Family Comparison



Examples: Pentium 510/60; 735/90; 815/100

THE iCOMP(TM) INDEX

- A NEW WAY TO COMPARE CPU PERFORMANCE
- iCOMP (**I**ntel **CO**mparative **M**icroprocessor **P**erformance).
- The iCOMP index is a simple numerical index of relative performance for making straightforward comparisons of Intel CPU power. It provides consumers with useful information when they make a PC purchase. It is intended to supplement, not replace benchmarks.
- The iCOMP formula was designed to reflect the full capabilities of a CPU--those which are executed not only by today's desktop systems and software applications, but the software expected to be in use throughout the three to five year average life of a system bought today.
- It is an index that reflects the relative performance of one Intel microprocessor to another, **not system performance**.

THE iCOMP(TM) INDEX

- The base processor for the iCOMP index is the 25-MHz Intel486 SX microprocessor, which has been assigned a value of 100. All other rated CPUs will have a number that is either above 100, meaning a faster CPU, or below, meaning slower.
- The size of the disparity between any two indices provides a relative measure of how much more powerful one CPU is than any other.
- However, to using the analogy of the EPA's highway and city mileage rating, the actual performance the user sees in the system depends on the individual car (system) and driving habits (specific types of software) of the user, as well as on the CPU.

Typical System Buses

Typical System Buses

The following pages describe the numerous bus standards implemented in today's Personal Computers.

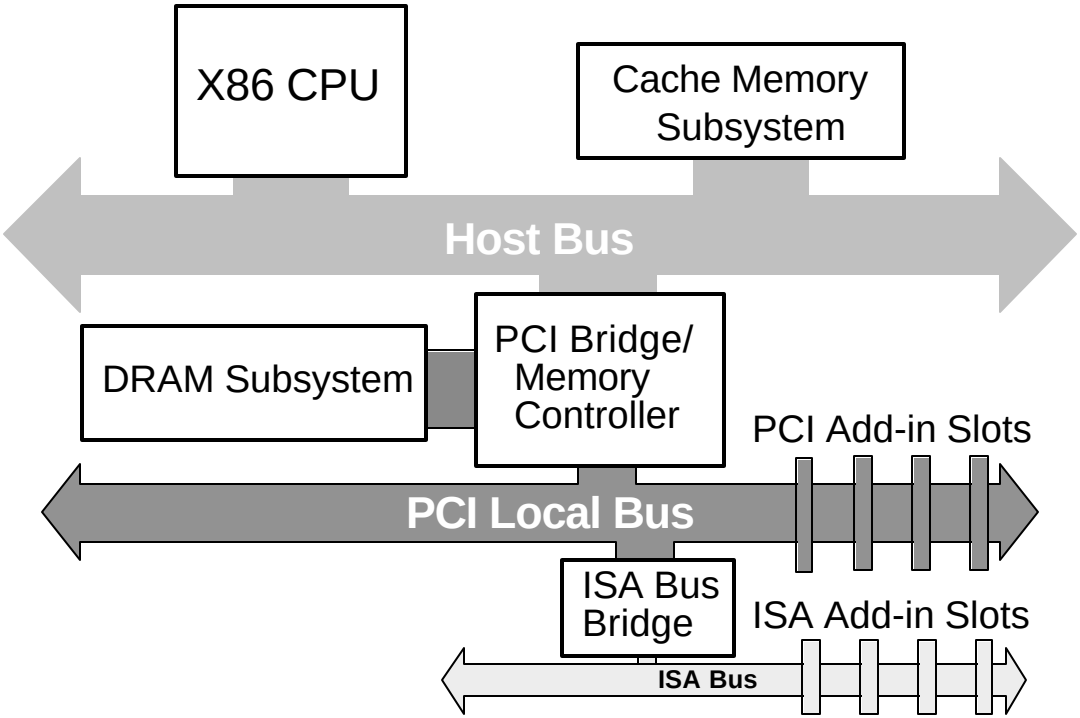
What is a Bus?

A ***bus*** is an electrical conduit in a computer that connects various components so they can communicate with each other.

A ***bus standard*** is a set of rules that govern *how* the communications will take place....think of it as "grammar" for a computer. And different bus standards will have different grammatical rules that affect how quickly they can communicate.

Typical System Buses

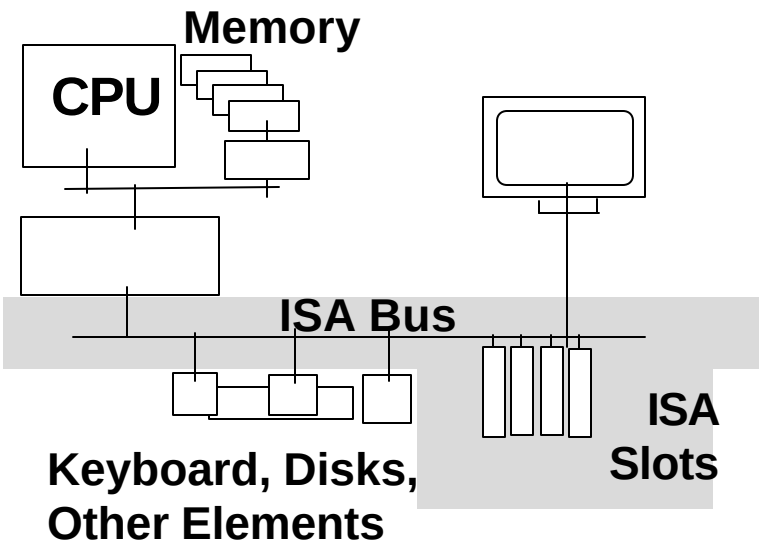
- "Bridges" isolate buses electrically and logically.
- Higher performance functions on PCI bus.
- Low performance functions on ISA or EISA bus.



Introduction - Bus Standards

ISA

When the PC was introduced in the early 1980's, the Industry Standard Architecture (ISA) bus was used. As the PC's popularity spread and "clones" appeared, the ISA bus was always used for compatibility. It is 16-bits wide at 8MHz, and is fully compatible with all PC software. An ISA system will accept ISA add-in cards It is found in most PCs.

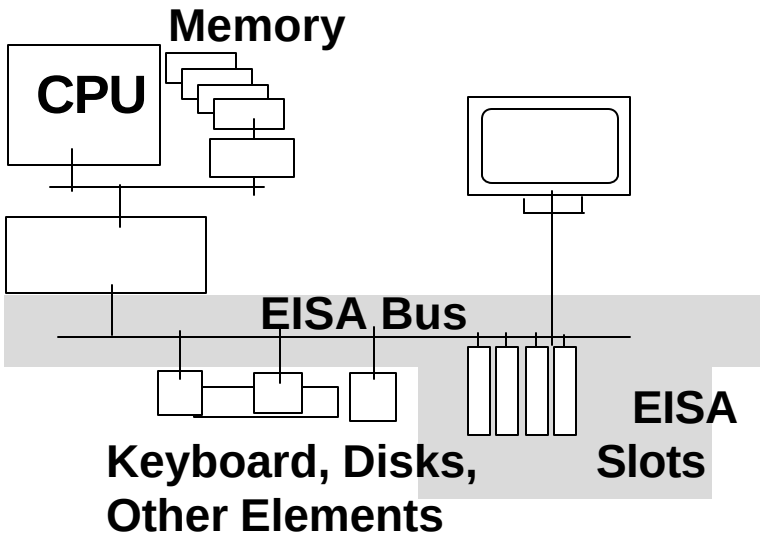


ISA Bus: Standard System

Introduction - Bus Standards

EISA

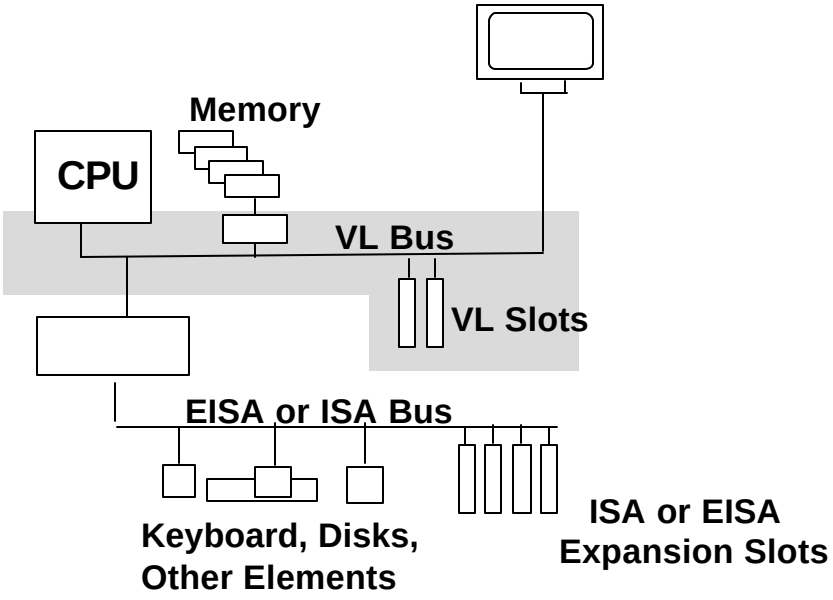
The **Enhanced ISA**, or EISA bus, is faster than ISA (32-bits @ 8MHz), and is fully compatible with ISA and all PC software. An EISA bus will give better overall performance to a computer system, and will accept ISA & EISA cards. It is typically used in servers, workstations and high-end PCs.



EISA Bus: Improved overall performance

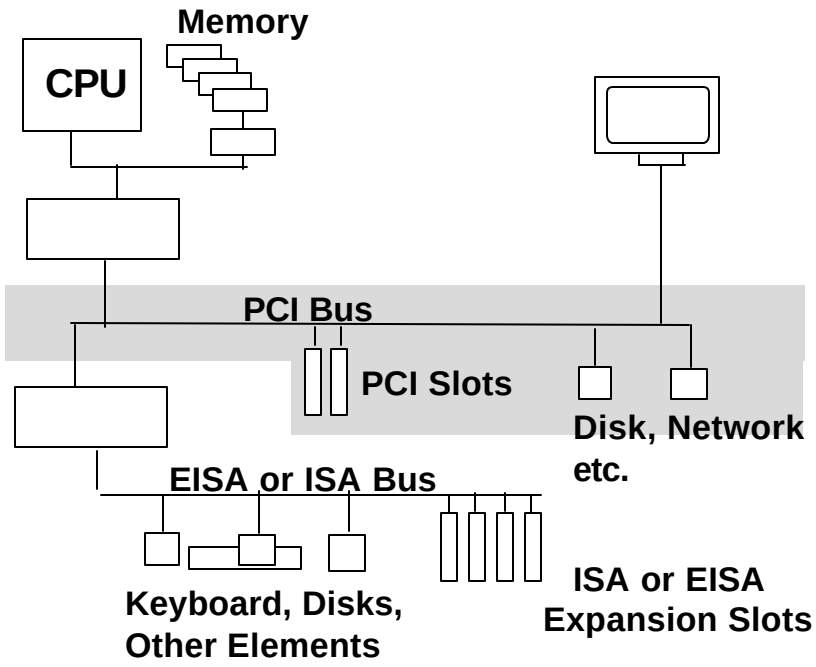
Introduction - Bus Standards

VL / VESA Local Bus: In 1992, the VL Local Bus began to appear and was mainly used to increase the graphics performance. It is used in conjunction with an ISA bus. Since the VL Bus is attached directly to the CPU, both must run at the same speed. For electrical reasons, the VL Bus can only support 2 add-in cards at 33MHz, and none at 50MHz.



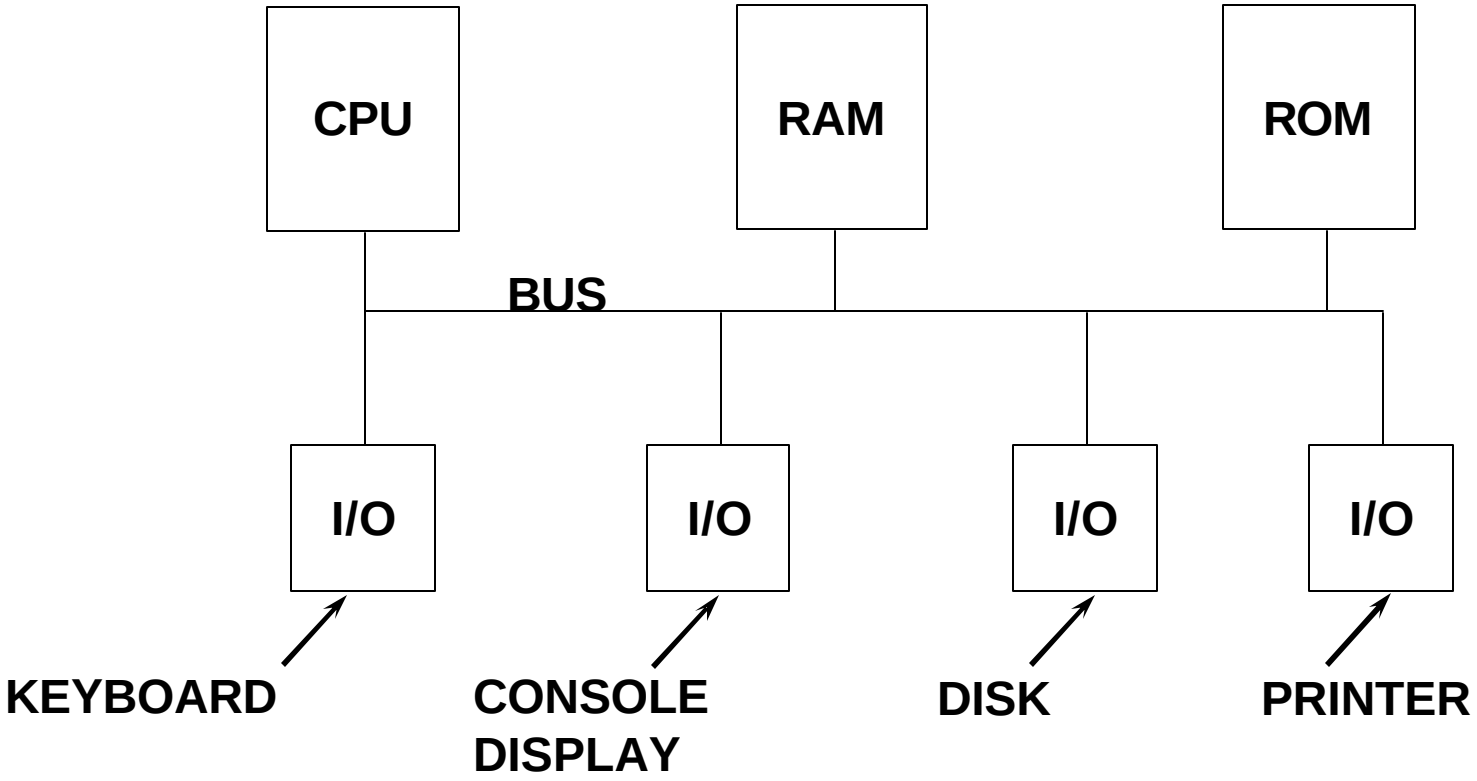
Introduction - Bus Standards

PCI Bus: Like the VL Bus, PCI will improve graphics performance, but will support other components as well (network, hard drive, etc.). Since it is not directly connected to the CPU, it sheds the electrical limitations of the VL bus and will accept multiple PCI-bus add-in cards.



Simple Microprocessor Systems

Simple Microprocessor Systems



Simple Microprocessor Systems

What are the needs of a simple microprocessor system?

- **A microprocessor**
- **Memory for program and data storage**
  - RAM--**R**andom-**A**ccess **M**emory comes in two main types:
    - DRAM--dynamic RAM; needs periodic refreshing
    - STATIC--fast, expensive; needs no refreshing
  - RAM does not retain the stored code and data when the computer is turned off. RAM is used to store the operating system and user programs.

Simple Microprocessor Systems

What are the needs of a simple microprocessor system? (Cont.)

- **ROM--Read-only memory-available in many main types**
  - PROMS--cannot be reprogrammed, but are cheaper
  - EPROMS--can be erased and reprogrammed (UV)
  - EEPROMS--can be erased and reprogrammed (byte at a time)
  - FLASH-- can be erased and reprogrammed (all cells at once)

- ROM retains the stored code and data when the computer is turned off. **ROM usually contains the following:**
  - POST--**P**ower-**O**n-**S**elf-**T**est
  - BIOS--**B**asic **I**nput **O**utput **S**ystem. Low level interface to devices (Low level I/O drivers and services).

Simple Microprocessor Systems

What are the needs of a simple microprocessor system? (Cont.)

- **I/O devices to provide user interaction with the computer. Typical I/O devices are these:**
  - **keyboard**
  - **display unit**
  - **file storage (floppy and hard disks)**
  - **printer**
  - **modems**

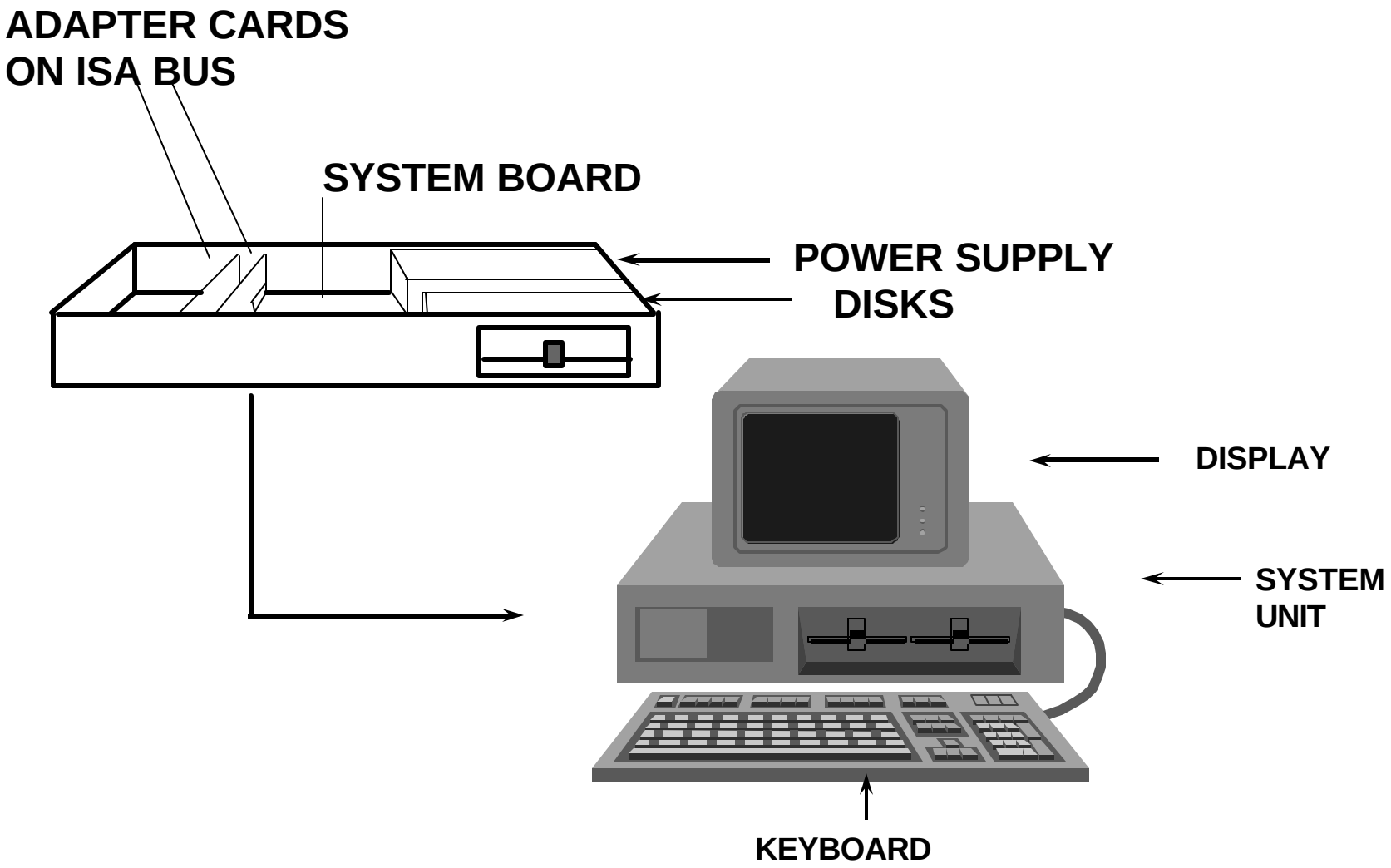
Statistical Comparison

	PCAT Compatibility Standard				
CPU	8088	80286	80386	80486	Pentium
Addr -BUS	20	24	32	32	32
MEM SIZE	1 MEG	1 6 MEG*	4 GIG *	4 GIG*	4 GIG*
VIRTUAL SIZE	NA	1 GIG	64 TERA	64 TERA	64 TERA
D-BUS	8	16	32	32	64
REG SIZE	16	16	32	32	32
# SEG. REGS	4	4	6	6	6
MATH	8087	80287	80387	On Chip	On Chip
BUS SPEED (MHz)	4.77, 10	8, 12	25, 33	33, 50	50, 60, 66
PAGING	NO	NO	YES	YES	YES
ON CHIP CACHE	NO	NO	NO	YES	YES

* Protected Mode

System Board Overview

PC/AT System Board Overview



System Board Overview

- The emphasis in this course is an Intel system board.
- The Intel system board is compatible with the original 8 MHz IBM PC/AT.
- We will use the term "PC/AT" to refer to a "generic" computer when we are not discussing specific implementations.

The following items define a PC/AT:

- A system board containing an Intel 80286, 80386, 80486 or Pentium microprocessor, plus peripheral chips compatible with the original IBM PC/AT.
  - » (The PC/XT used an Intel 8088.)
- System board "adapter card slots" (ISA) compatible with those on the original IBM PC/AT.
- Disk drives providing IBM PC/AT compatibility (diskette and fixed disks).

System Board Overview

- The following items define a PC/AT: (Cont.)
  - A power supply (+5v, -5v, +12v, -12v).
  - A compatible keyboard.
  - A display adapter and monitor. The basic types are monochrome, CGA, EGA, and VGA.
  - The system board must contain an IBM PC/AT compatible BIOS. Examples are AMI, Award and Phoenix BIOS.
    - Many applications directly access low-level hardware and BIOS functions. This leads to requirement that the board must contain an IBM PC/AT compatible BIOS.
  - In addition to connecting the above components, a PC/AT must be able to run MS DOS or PC DOS applications.

System Board Overview

- **Add-on products typically come with software drivers and adapter cards. Examples include:**
  - **Printers**
  - **Diskette and fixed disk controllers and drives**
  - **Communications (RS232, LANS, GPIB, Modems)**
  - **Mice**
- **NOTE: IBM has published Technical References for the IBM PC, PC/XT, and PC/AT.**
  - The references include circuit diagrams and BIOS listings and provide the information necessary for the PC industry to produce imitations.
  - The references were not complete, as they didn't adequately define the (ISA) bus signals.

THE SYSTEM BOARD IN DETAIL

MICROPROCESSOR

- The original PC/AT contained the following chips which formed the heart of the system board:
  - an Intel 80286 microprocessor (6 then 8 MHz)
  - an Intel 82284 clock, reset, and ready chip
  - an Intel 82288 bus controller chip
  - a socket for the Intel 80287 math coprocessor

- Current Intel boards have contain a microprocessor and a ChipSet which incorporates the functions of the the Bus & Memory Controllers as well as most of the peripheral chips.

THE SYSTEM BOARD IN DETAIL

BUSES

- On the original PC/AT, several "buses" were created from the local 286 bus. Each bus, including the 286 local bus, has three parts **(address, data, control)**
- **Current Intel boards have buses that contain the three basic parts (address, data, control).**

SYSTEM BOARD RAM MEMORY

- The system board of the IBM PC/AT contained up to 512K bytes of dynamic RAM. Adapters could be added to bring the memory to 640K bytes and above.
- Current Intel boards contain upwards of 128M on the system board (using SIMM or DIMM modules).

XT, AT System Board Peripherals

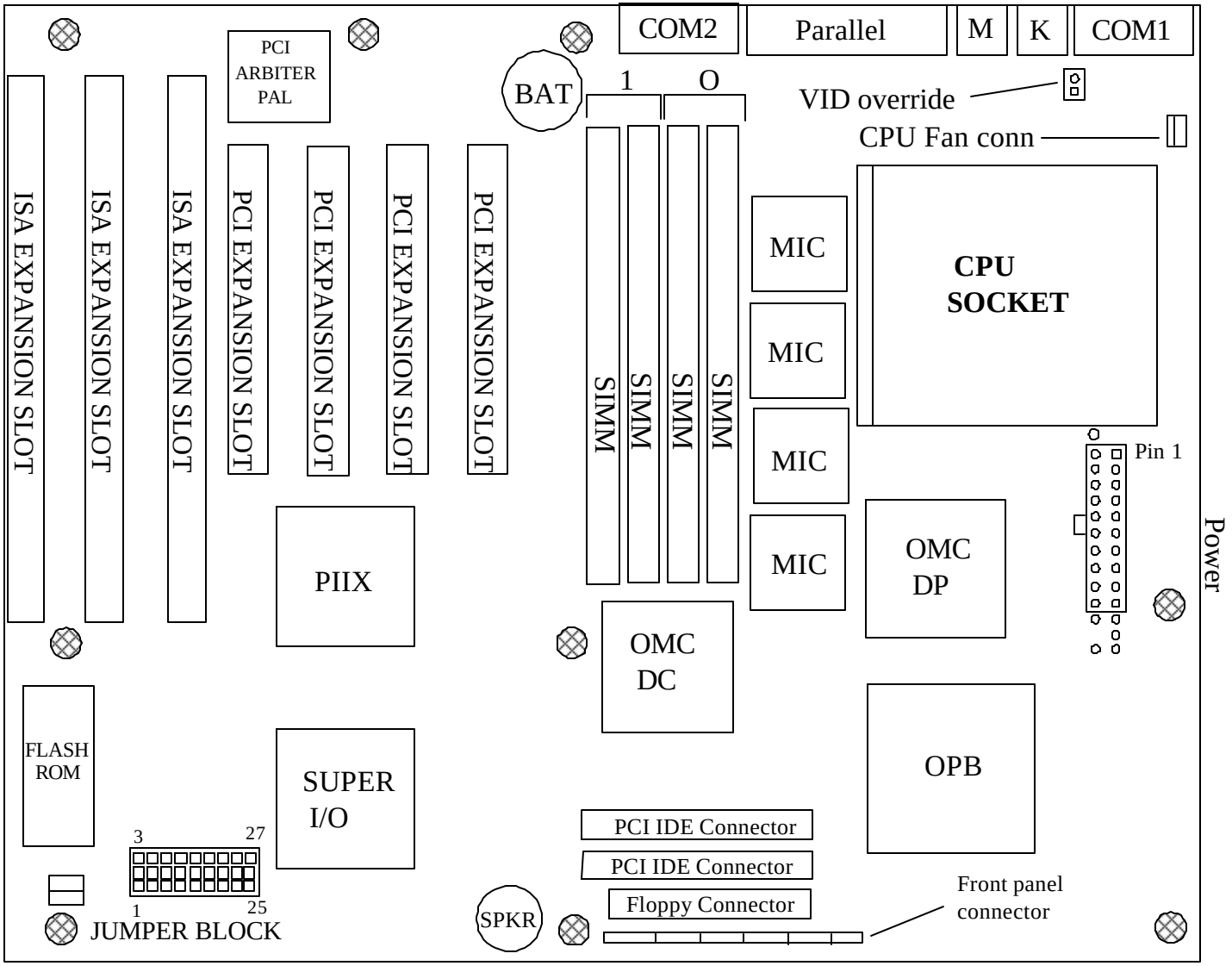
Today's Personal Computers are COMPATIBLE with the PC/A

	XT	AT		
CPU	8088	80286	80386	80486 & Pentium
MATH	8087	80287	80387	on Chip
TIMER (pit)	8253	8254		
DMA	8237	2 - 8237s		
INTERRUPTS (pic)	8259	2 - 8259s		
DIGITAL I/O	8255	LOGIC 8042 Micro controller		
RAM	640K	16MEG	Up to 4 GIG	
ROM	48K	64K (128K)		
REAL-TIME CLOCK	NONE	CLOCK CHIP W/ CMOS RAM BATTERY BACKUP		

XT, AT System Board Peripherals

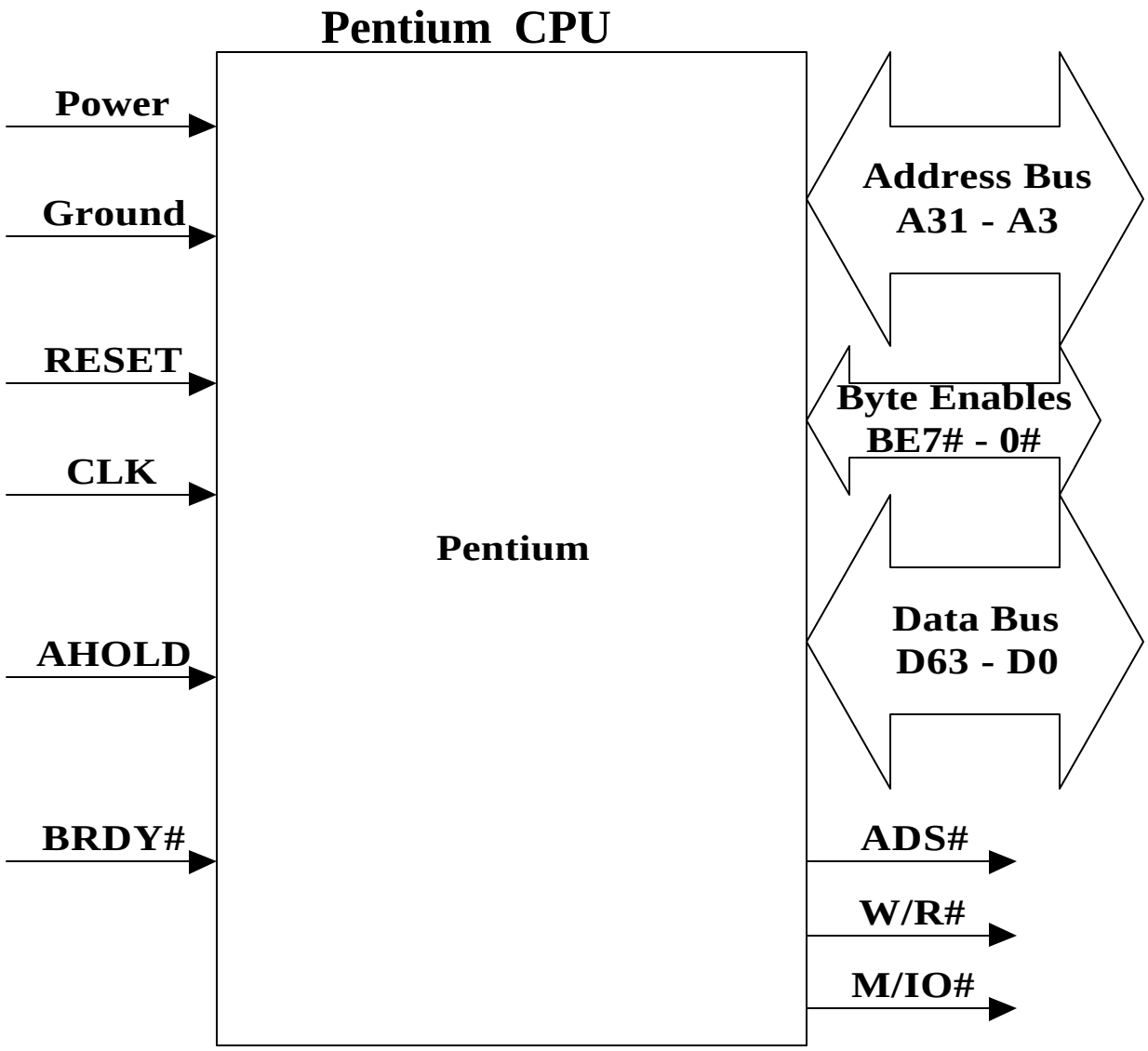
- **SYSTEM BOARD PERIPHERAL CHIPS: These will be described in detail in this course.**
  - An Intel 8254 **P**rogrammable **I**nterval **T**imers (PIT).
  - Two Intel 8259A **P**rogrammable **I**nterrupt **Cont**roller chips (PIC).
  - An Intel 8042 (8742) MICROCONTROLLER to provide digital I/O and to interface with the keyboard.
  - A real-time clock chip that provides time, and 64 bytes of CMOS RAM for configuration information. The clock chip is backed up with a battery.
  - Two Intel 8237-5 DMA Controller chips.
  - A 74LS612 latch to provide page information during DMA transfers.
  - A DRAM Refresh Controller.
- Remaining system board features (not covered in this course)
  - Two 82510 (or compatible) UARTS providing two COM ports.
  - Circuitry to support a parallel printer port.
  - A speaker for beeping.

System Board Component Layout



Microprocessor Buses & Simple Bus Cycles

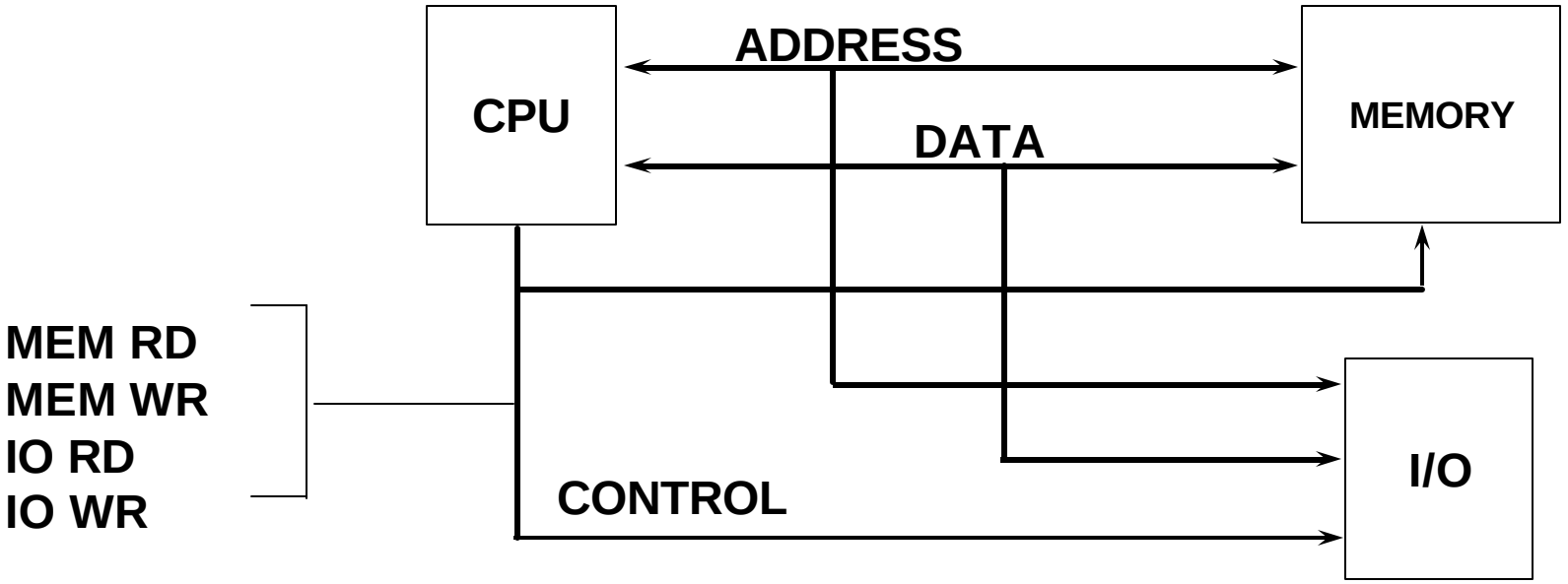
CPU Signals Required for operation



CPU Signals Required for operation

- Power and Ground signals on multiple pins.
  - 5.0v for P5, 3.3v for P54C
- Processor RESET (input):
- Processor CLOCK (input): Often 50, 60, or 66 MHz depending on design.
- AHOLD (input) not active: Used to disable the address bus for alternate bus master (e.g. DMA) cache snooping.

Microprocessor Buses



MICROPROCESSOR BUSES

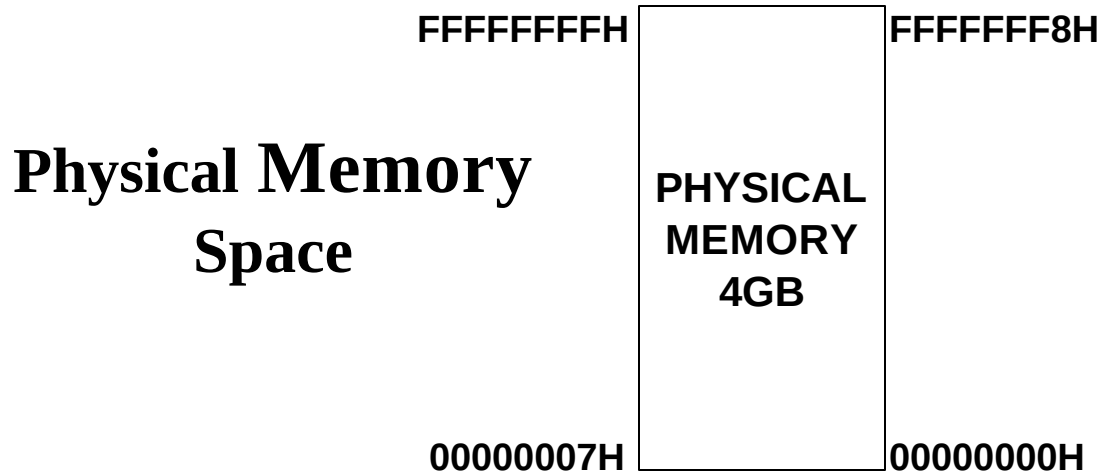
- The microprocessor uses several buses to communicate with memory and I/O.

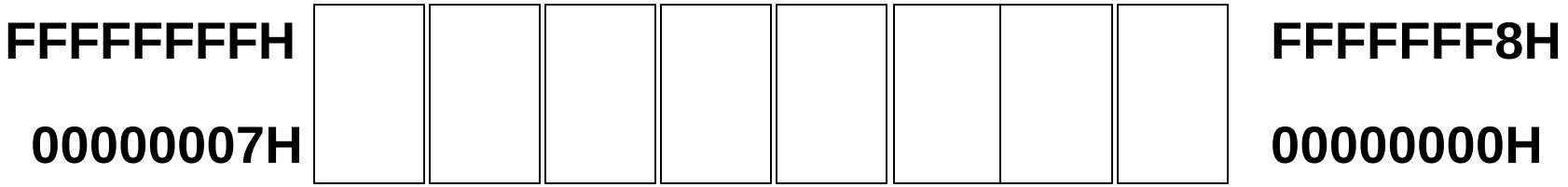
- In general, there are three buses:
  - Address
  - Data
  - Control

MICROPROCESSOR BUSES

- **Address bus:** The microprocessor provides an address to the memory & I/O chips.
  - The number of address lines determines the amount of memory supported by the processor.
  - **A31:A3** Address bus lines determines where in the 4GB memory space or 64K IO space the CPU is accessing.
  - **BE7#:BEO#** (outputs): Byte enable lines to enable each of the 8 bytes in the 64-bit data path.
    - In effect a decode of the address lines A2-A0 which the Pentium does not generate.
    - Which lines go active depends on the address, and whether the cycle requires a byte, word, double word or quad word.

Bus Description

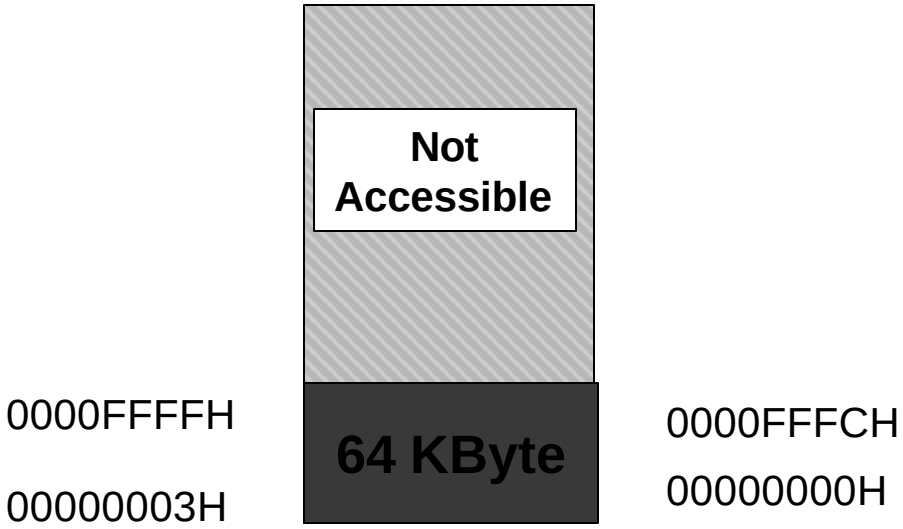




64-BIT Wide Memory Organization

Bus Description

- I/O Address Space is limited to 64 Kbytes (0000H-FFFFH).
- This limit is imposed by a 16 bit CPU Register.
  - A 16 bit register can store up to FFFFH (1111 1111 1111 1111 y).



I/O Space

MICROPROCESSOR BUSES

Data bus: The data bus provides a path for data to flow.

- The data can flow to/ from the microprocessor during a memory or I/O operation.
  - Provides the propagation path in both directions.
- **D63:DO** (bi-directional): The 64-bit data path to or from the processor.
  - The signal W/R# distinguishes direction.
- Parity **DP7:DPO** (bi-directional): Pentium uses **EVEN** parity bits on a per-byte basis.
  - Parity signals: Output on writes, Input on reads.
    - Not supported on all systems.

MICROPROCESSOR BUSES

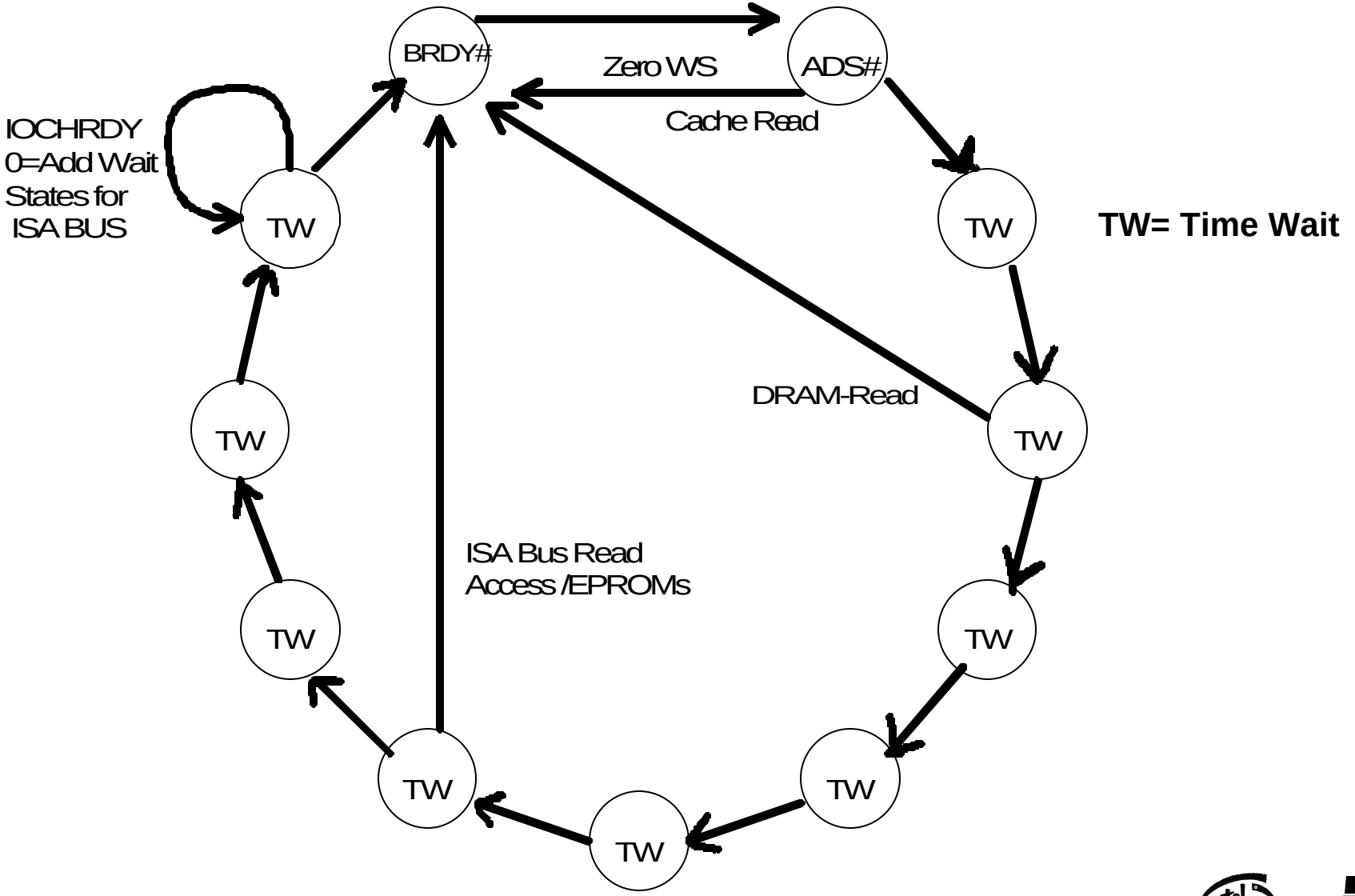
Control bus: The control bus is used by the microprocessor to tell the memory and I/O chips what the microprocessor is doing.

- Typical control bus signals are these:
  - **M/IO#** (output): Defines if the bus cycle is a Memory access or an IO Port access.
  - **D/C#** (output): Defines if the bus cycle is Data or Code for Memory access.
  - **W/R#** (output): Indicates if bus cycle is a Write or a Read operation.
  - **Cache#**. (output): Processor indication of internal cacheability. Cache# and Ken# are used together to determine if a read will be turned into a linefill. (Burst cycle).

MICROPROCESSOR BUSES

- **CONTROL BUS (Cont)**
- **ADS#** (output): Signals that the processor is beginning a bus cycle.
  - From power-on the ADS# signal should be asserted periodically when bus cycles are running.
- **BRDY#** (input): This signal ends the current bus cycle (low) and is used to extend bus cycles (high) to allow slow devices extra time.
  - If LOW, this signal ends the current bus cycle and the next bus cycle can begin.
  - If HIGH the Pentium is prevented from continuing processing and wait states are added to allow slow devices extra time.

Ready Logic State Machine Example



Microprocessor Bus Cycles

- A BUS CYCLE begins with the Processor driving an address and control signals and asserting ADS#.
- A BUS CYCLE ends when the last BRDY# is returned to the Processor.
- A BUS CYCLE may have 1 or 4 data transfers.
  - A SINGLE Cycle transfer is 64 bits maximum [8 bytes].
  - A BURST Cycle transfer is 256 bits (4*64) [32 bytes]
- The following table lists all the bus cycles that will be generated by the Pentium microprocessor
  - (From Table 6-10 in Pentium manual)

Bus Cycle Definition

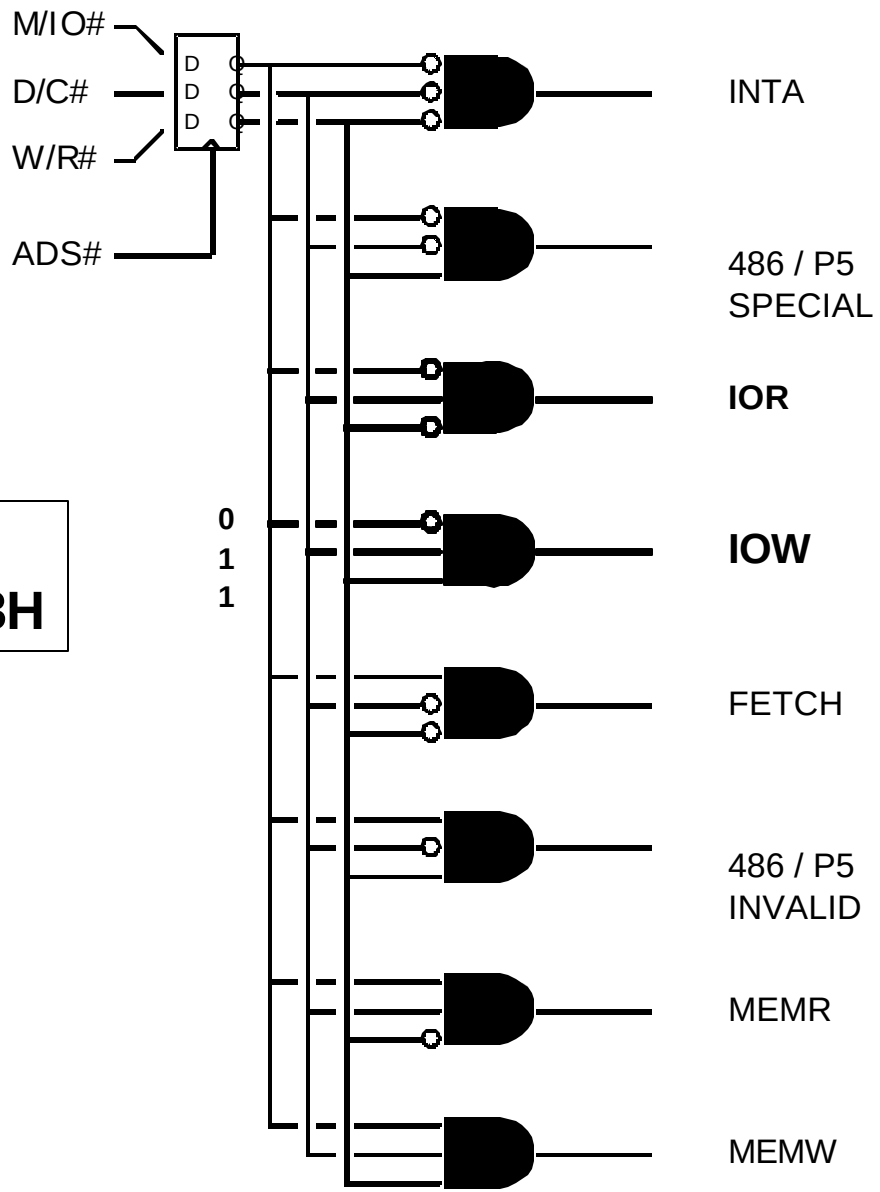
M/IO#	D/C#	W/R#	Cache#	Ken#	Cycle Description	No. of Transfers
0	0	0	1	x	Interrupt Acknowledge (2 locked cycles)	1 transfer each cycle
0	0	1	1	x	Special Cycle	1
0	1	0	1	x	I/O Read . 32-bits or less Non Cacheable	1
0	1	1	1	x	I/O Write . 32-bits or less Non Cacheable	1
1	0	0	1	x	Code Read. 64-bits. Non Cacheable	1
1	0	0	x	1	Code Read. 64-bits. Non Cacheable	1
1	0	0	0	0	Code Read . 256-bit burst Line Fill	4
1	0	1	x	x	Intel Reserved (will not be driven by the Pentium™ processor).	n/a
1	1	0	1	x	Memory Read. 64 bit or less. Non Cacheable	1
1	1	0	x	1	Memory Read. 64 bit or less. Non Cacheable	1
1	1	0	0	0	Memory Read. 256 bit bursrt Line Fill	4
1	1	1	1	x	Memory Write. 64 bit or less Non Cacheable	1
1	1	1	0	x	256 bit Burst Write back	4

*Cache# will not be asserted for any cycle in which M/IO# is driven low, or for any cycle in which PCD is driven high.

GENERIC DECODE LOGIC

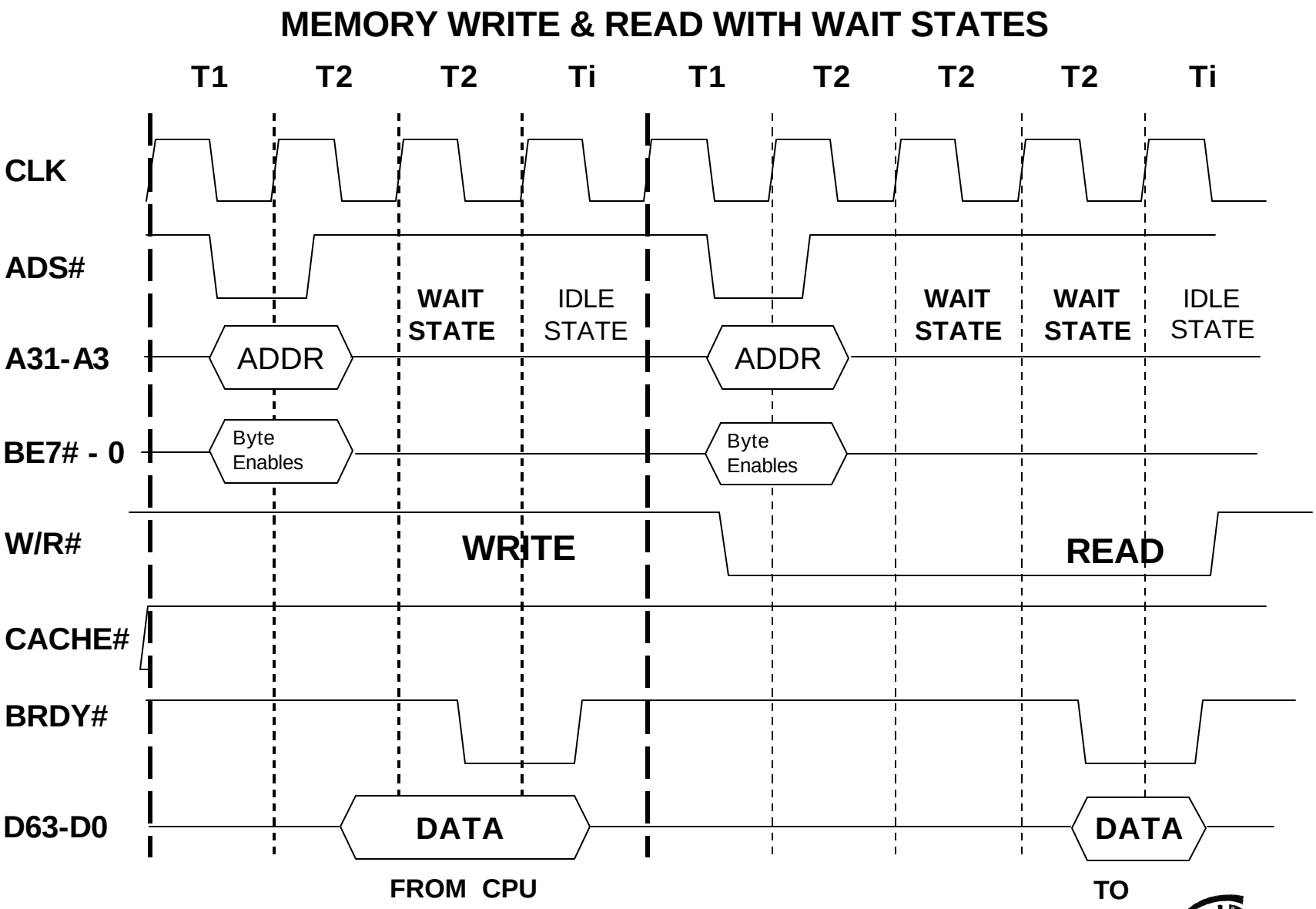
- The system board contains some logic to decode the BUS CYCLE DEFINITIONS of the CPU.
- The BUS CYCLE DEFINITIONS from the CPU are VALID when ADS# is asserted (Logic 0).
- The drawing shows an example of logic that could be used to decode the BUS CYCLE DEFINITIONS.
- The signals generated by the GENERIC DECODE LOGIC would be used by the System Board to generate signals such as I/O chip selects and DRAM & PROM output enables.

GENERIC DECODE LOGIC

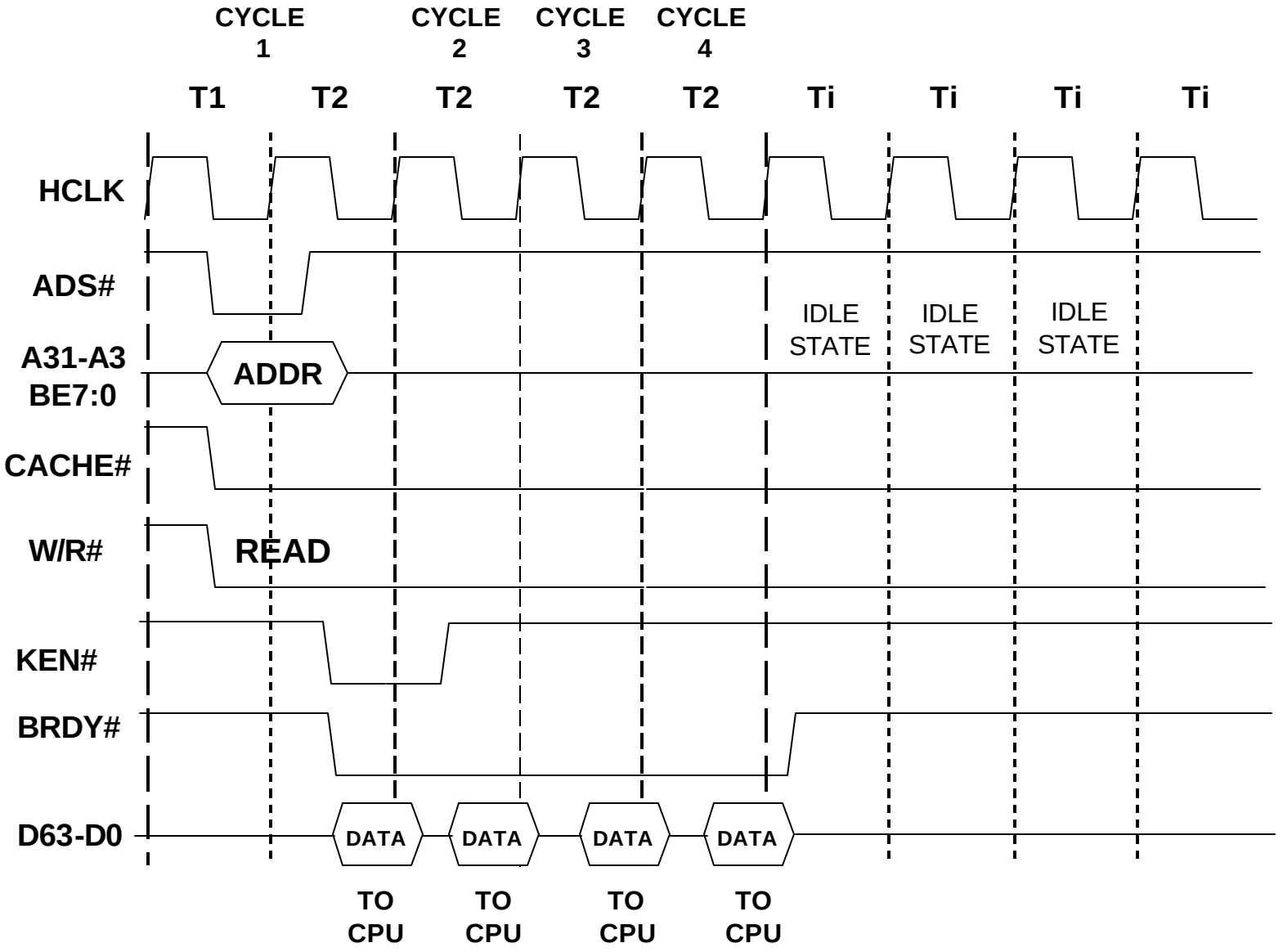


e.g.
I/O WR @ Addr 43H

Microprocessor Single Bus Cycle

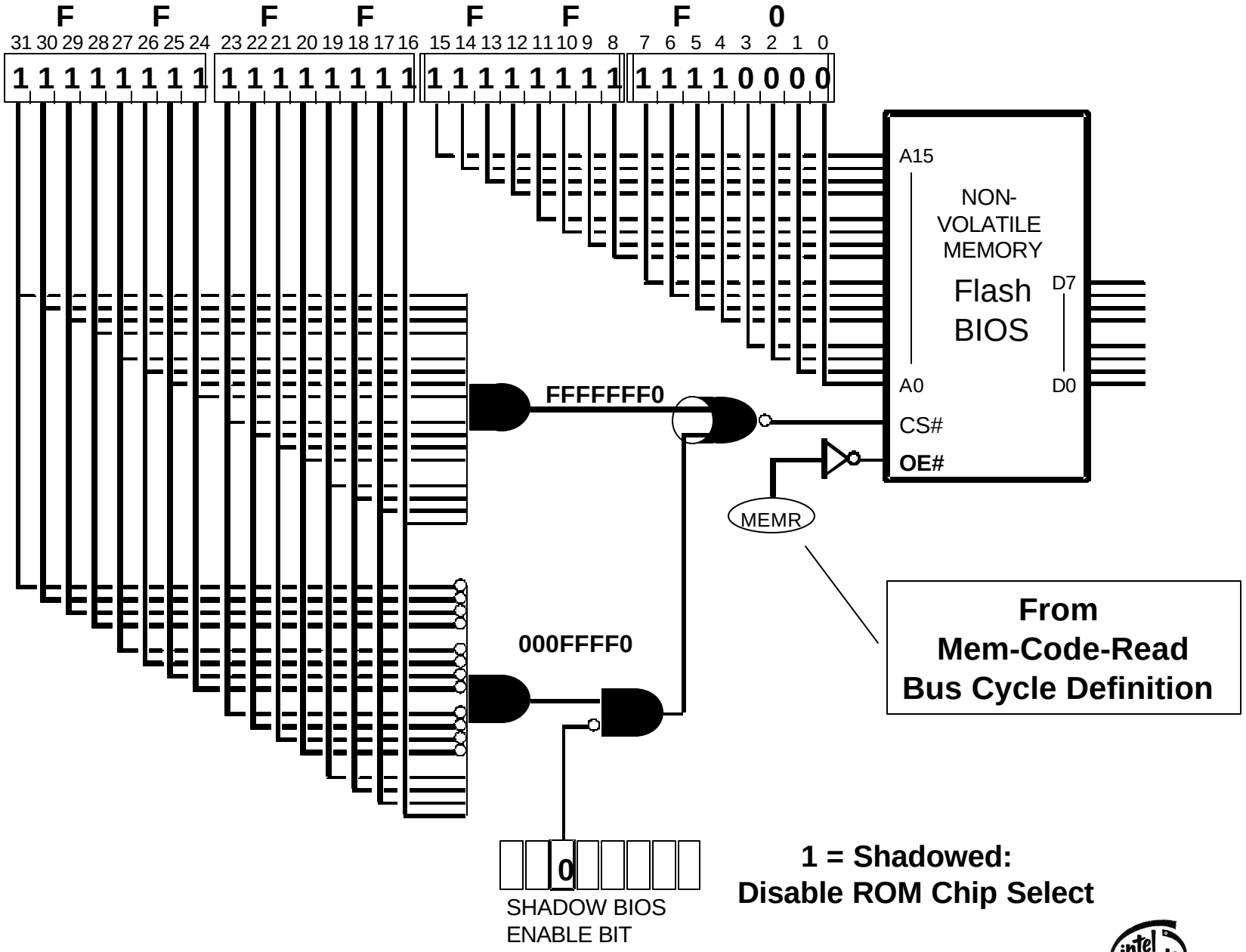


Basic Burst Read Cycle



Fetching the Initial Instructions

ACCESSING THE BIOS


F F F F F F F 0
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0 0 0 0
A15
NON-
VOLATILE
MEMORY
Flash
BIOS
D7
D0
A0
CS#
OE#
FFFFFFF0
000FFFF0
MEMR
From
Mem-Code-Read
Bus Cycle Definition
0
SHADOW BIOS
ENABLE BIT
1 = Shadowed:
Disable ROM Chip Select

ACCESSING THE FLASH BIOS

- The **Chip Select** for the BIOS is the result of **decoding** the **Reset Vector.**
  - The **CPU Address at Reset** is the Reset Vector.
    - **Address = FFFFFFF0 physical**. The physical address is the output on the CPU address bus.
  - The Upper AND GATE will generate a **CS#** for address **FFFFXXXXp**
- The **Mem Code Read** bus cycle definition causes the Flash BIOS **Output Enable**.
  - The first bus cycle definition is a Code Fetch
    - (Memory, Code, Read)

Fetching the Initial Instructions

- The CPU is forced into a known condition at RESET.
  - The address is set to the Reset Vector (FFFFFFF0 physical)
    - CPU internal registers generate this address.
  - The first bus cycle definition is a Code Fetch.
- The CPU will **FETCH** the first instructions from the BIOS.
  - The ROM BIOS is chip selected as a result of the Reset Vector address (FFFFFFF0)
  - The Flash BIOS output enable results from the Mem Code Read bus cycle definition.
  - The ROM data is accepted by the CPU when BRDY# is asserted.

Fetching the Initial Instructions

- The CPU **DECODE**S the ROM BIOS instructions.
  - The HEX BYTES (machine code) stored in the BIOS are decoded by the CPU into instructions.
- The first instruction decoded is a FAR JUMP to 000**FEO5B**p
  - The F0000p-FFFFFp range is the 1 MB COMPATIBLE PC/AT address range accessed in REAL MODE.
  - BIOS Chip Select now results from decoding 000FEO5Bp.
  - The Lower AND GATE will generate a **CS#** for an address in the **000FXXXXp range** (000F0000p - 000FFFFFp).
- POST will now **EXECUTE** in the F0000p-FFFFFp range

Fetching the Initial Instructions

- The CPU executes the Code fetched from the ROM and the POST (**P**ower **O**n **S**elf **T**est) is executed.
  - POST detects, checks, & initializes installed components on the system board.
  - **POST** writes a **CODE** to I/O **Port 80** at the **start** of each new POST test.
  - POST normally stops on critical Failures.
    - The LAST POST CODE written to Port 80 is an indication of the failure.
  - If everything is OK, POST gives control to a Bootstrap Loader to load an Operating System via INT 19H.
- The majority of failures will occur before POST has completed and gives control to a Bootstrap Loader .

SUMMARY

WE HAVE DISCUSSED THE FOLLOWING:

- THE **iCOMP**(TM) INDEX
- System Buses.
- Simple Microprocessor Systems
- The System Board & Peripheral chips.
- Microprocessor Buses & simple bus cycles.
- Fetching instructions after CPU is reset.